

Docket No.: J&R-0694

MAR 10 2006

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Werner H. SternerMarch 10, 2006
DateIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	09/922,479	Confirmation No:	7212
Applicant	:	Thomas Zettler		
Filed	:	August 3, 2001		
Title	:	Method and Device for Testing an Integrated Circuit, Integrated Circuit to be Tested, and Wafer with a Large Number of Integrated Circuits to be Tested		
Art Unit	:	2138		
Examiner	:	Phung M. Chung		
Docket No.	:	J&R-0694		
Customer No.	:	24131		

RESPONSE

Hon. Commissioner for Patents


Sir:

Responsive to the Office Action dated February 13, 2006, the following remarks are made:

In deference to the restriction requirement on page 2 of the above-identified Office Action, applicants elect group I, claims 1 - 4, 6 - 17, 19 - 23 and 29 for prosecution at this time.

In view of the foregoing, the early issuance of an Action on the merits of claims 1 - 4, 6 - 17, 19 - 23 and 29 is solicited.

Respectfully submitted,


Werner H. Sterner (34,956)

Date: March 10, 2006

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